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| <b>TRANSMITTAL FORM</b><br>(to be used for all correspondence after initial filing) | Application / Conf. No. | 10/021,447 / 6106 |
|   | Filing Date             | October 30, 2001  |
|   | First Named Inventor    | Siuki Chan        |
|   | Examiner Name           | Aditya S. Bhat    |
|   | Art Unit                | 2863              |
|   | Patent No.              |                   |
| Mail Stop: A F  | Attorney Docket Number  | X-885 US          |
| Express Mail Receipt No.  |                         |                   |
| Total Number of Pages in This Submission  |                         |                   |

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| <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53  |  |  |
| Remarks   |  |  |

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X-885 US  
10/021,447

PATENT  
Conf. No. 6106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Siuki Chan  
Assignee: Xilinx, Inc.  
Title: Methods and Circuits for Measuring Clock Skew on  
Programmable Logic Devices  
Serial No.: 10/021,447 Filing Date: 10/30/2001  
Examiner: Aditya S. Bhat Art Unit: 2863  
Docket No.: X-885 US Conf. No.: 6106

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AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

In response to the Final Office Action mailed from the Patent Office on December 4, 2003, Applicant submits the following amendments and remarks.

**Amendments to the Claims** begin on page 2 of this paper.  
**Remarks** begin on page 8 of this paper.